SEMICONDUCTOR DEVICE AND METHOD OF SETTING INPUT PIN CAPACITY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor device having a semiconductor chip suitable for multi-chip package and a method of setting the capacity of an input pin for the semiconductor chip.

2. Description of the Related Art

Japanese Patent Application Number 10-321742 (hereinafter "related art") describes that although a single chip package having only one chip per package has been a main stream in the field of DRAM, a multi-chip package having a plurality of chips per package has been developed recently to meet the requirements of a large capacity DRAM.

The related art proposed that in a double mounted type semiconductor device, an electrostatic protection circuit was provided in either a single semiconductor chip or two decentralized semiconductor chips.

The input pin capacity of a DRAM is specified that, for example, the maximum value is 5 PF and the minimum capacity is 2.5 PF. The input pin capacity consists of the package capacity that is determined according to the factors of a package and the chip capacity that is determined according to the factors of chips.

Since the package capacity is more difficult to change than the chip capacity, the related art proposed to adjust the chip capacity to meet the specifications.

Fig. 14 shows a conventional input circuit of a semiconductor chip. N-channel MOS transistors are used in the related art; however, CMOS transistors are used in Fig. 14 for convenience of comparison with the present invention.

The input circuit comprises an electrostatic protection element 1, an input pad 2, and a wiring 3. The electrostatic protection element 1 is a capacitor of CMOS transistors in which a P-channel MOS transistor Pch and an N-channel MOS transistor Nch are connected to each other.

The electrostatic protection element 1 is provided so as to prevent an inner circuit from being broken down by a high voltage that is caused by static electricity through the input pad 2 and the wiring 3.

The chip capacity of the input pin capacity is the sum of junction capacities between a source and a drain of the P-channel MOS transistor Pch and the N-channel MOS transistor Nch. Since the chip capacity is in proportion to the junction area of the pn junction, the input pin capacity is determined by adjusting the junction area at the stage of design.

However, when a multi-chip package is developed using chips which have the chip capacity for a single chip package, the sum of the chip capacity exceeds the upper limit of the specified chip capacity for the multi-chip package because the specified input pin capacity of the multi-chip package is the same as that of the single chip package. The chip capacity is constant so that the added capacities were unable to be changed according to the number of the chips used in the multi-chip package.

BRIEF SUMMARY OF THE INVENTION

According to the invention, in order to solve the above problem, fuses are provided in the input circuit between the electrostatic protection elements and the wirings for connecting the input pad and the inner circuit and a predetermined fuse is disconnected according to the number of semiconductor chips mounted in the multi-chip package.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of an input circuit according to the first embodiment of the present invention.

Fig. 2 is a schematic diagram of the first embodiment of the invention.

Fig. 3 is a schematic diagram of an input circuit according to the second embodiment of the present invention.

Fig. 4 is a schematic diagram of the second embodiment of the invention.

Fig. 5 is a schematic diagram of an input circuit according to the third embodiment of the present invention.

Fig. 6 is a schematic diagram of the third embodiment of the invention.

Fig. 7 is a schematic diagram of an input circuit according to the fourth embodiment of the present invention.

Fig. 8 is a schematic diagram of the fourth embodiment of the invention.

Fig. 9 is a schematic diagram of the fifth embodiment of the invention.

Fig. 10 is a schematic diagram of the sixth embodiment of the invention.

Fig. 11 is a schematic diagram of the seventh embodiment of the invention.

Fig. 12 is a schematic diagram of the eighth embodiment of the invention.

Fig. 13 is a schematic diagram of the ninth embodiment of the invention.

Fig. 14 is a schematic diagram of a conventional input circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In Fig. 1, an input circuit comprises an electrostatic protection element 1, an input pad 2, wiring 3, and a fuse 4. The electrostatic protection element 1 is constructed such that the capacitor made by two P-channel

MOS transistors Pch-1 and Pch-2 that each has a half of the chip capacity of the input pin capacity, is equal to the conventional capacitor made by one P-channel MOS transistor Pch.

Similarly, N-channel MOS transistors Nch-1 and Nch-2 make a capacitor in the input circuit. Thus, the capacitors according to the invention are made by CMOS transistors. However, the capacitor made by only N-channel or P-channel MOS transistor may be used.

The input pad 2 is an input terminal which is connected to a pin, and the wiring 3 connects the input pad 2 and an inner circuit. The input pad 2 and the wiring 3 are identical to conventional ones. The fuse 4 is formed by the same material as a metal wire, such as aluminum, in the same way as for a wiring pattern. An additional element, such as a diode, may be included in the input circuit.

A first electrostatic protection element 1 formed by the transistors Pch-1 and Nch-1 is connected to the wiring 3. A second electrostatic protection element 1 formed by the transistors Pch-2 and Nch-2 is disposed in the vicinity of the wiring 3. The fuse 4 is provided between the wiring 3 and the second electrostatic protection element 1.

The transistors Pch-1 and Pch-2 have equal capacitance. That is, the chip capacity of the input pin capacity of the package is divided equally into the two by dividing a half, the pn junction area between the source and drain at the stage of design. The same thing is applicable to the capacity formed by the transistors Nch-1 and Nch-2.

When a semiconductor chip comprising the above-described input circuit is used in single chip package, only one chip formed by the transistors Pch-1, Pch-2, Nch-1,

and Nch-2 is mounted in a package. In the single chip package, since the fuse 4 is not disconnected, the second electrostatic protection element 1 formed by the transistors Pch-2 and Nch-2 is electrically connected to the wiring 3.

In Fig. 2, in the multi-chip package (two chip are mounted in a package), the fuses 4 are disconnected to electrically disconnect the second electrostatic protection element 1 formed by the transistors Pch-2 and Nch-2 so that only the first electrostatic protection element 1 formed by the transistors Pch-1 and Nch-1 is used.

In the multi-chip package, the respective input pads 2 of the two chips having the disconnected fuse 4 are connected to a common terminal 5. Then, the two chips are mounted in the package to make the semiconductor device of the multi-chip package.

When the two semiconductor chips each having the chip capacity of a half value and the disconnected fuses 4 are mounted in the package, the input pin capacitance of the package does not exceed the upper limit of the specification.

The disconnection of the fuse 4 is performed by laser after the treatment of a wafer. It is recommended that the pattern width of the fuse 4 is made small or the pattern film is made thin so that the disconnection is made easy.

In Fig. 3, the second embodiment of the invention has the same structure as in the first embodiment except that the first electrostatic protection element 1 formed by the transistors Pch-1 and Nch-1 is also connected to the wiring 3 through the fuse 4.

It is required that at least one of the electrostatic protection elements 1 is connected to the input pad 2 to prevent the breakdown of the inner circuit.

In the second embodiment, all of the electrostatic protection elements 1 are connected to the wiring 3 through the respective fuses 4 so that any fuse 4 can be disconnected.

In Fig. 4, one of two pairs of the fuses 4 of each chip in the multi-chip package is disconnected and the other pair of the fuses 4 are not disconnected so that the corresponding electrostatic protection element 1 is electrically connected to the wiring 3 through the fuses 4.

In the first and second embodiments, two chips are mounted in a package. In the third embodiment shown in Figs. 5 and 6, the chips in the number of n are mounted in a package (n is an integer larger than 2). In the chips for the third embodiment, the fuses 4 are provided for all the electrostatic protection elements 1 except for the first electrostatic protection element 1.

In the third embodiment, the chip capacity is equally divided into the number of n. That is, the junction areas of the respective transistors Pch-1 to Pch-n are set at 1/n of the junction area of the conventional transistor Pch for the single chip package. Similarly, the junction areas of the respective transistors Nch-1 to Nch-n are set at 1/n of the junction area of the conventional transistor Nch.

When this semiconductor chip is used in the single chip package, one chip is mounted in a package without disconnecting any fuses 4 so that the electrostatic protection elements 1 in the number of n (from the first to n-th electrostatic protection elements 1) are electrically connected to the wiring 3.

In Fig. 6, when this semiconductor chip is used in the multi-chip package, the chips in the number of n are mounted in a package with disconnecting all pairs of the fuses 4 so that the electrostatic protection elements 1 in

the number of n-1 (from the second to n-th electrostatic protection elements 1) are electrically disconnected from the wiring 3 and only the first electrostatic protection element 1 is electrically connected to the wiring 3. The respective input pads of the chips in the number of n are connected to the common terminal 5 of the package.

In Fig. 7, the chip for the fourth embodiment has the same structure except that the first electrostatic protection element 1 is also provided with a pair of the fuses 4 so that the transistors Pch-1 and Nch-1 are connected to the wiring 3 through the fuses 4.

In Fig. 8, when the chip is used for the multi-chip package, all the pairs of the fuses 4 are disconnected but only the pair of fuses 4 of the first electrostatic protection element 1 is not disconnected. It is easy to determine which pair of the fuses 4 is disconnected, by changing the program for the disconnection by laser. Accordingly, it is not necessary that the fuses 4 of the first electrostatic protection element 1 is always used, but any pair of fuses can be used.

In the fourth embodiment, the first electrostatic protection element 1 is not disconnected. In the fifth embodiment (Fig. 9), however, the fuses 4 of the first and second electrostatic protection elements are disconnected and the fuses 4 of the third to s-th electrostatic protection elements 1 are disconnected. The respective pads 2 are connected to the common terminal 5 of the package.

When the chips in the number of n are mounted, it is necessary that the chip capacity of the input pin capacity of each chip is divided by the number of s which is larger than n, for example, 2n. Otherwise, there is the risk that the multi-chip package has the input pin capacity exceeding the specification.

When the chips in the number smaller than n, for example, n-1, are mounted, the chip capacity of the input pin capacity may be divided by s (=n). In any case, it is required to meet the specification of the input pin capacity of the package. The transistors Pch-1 and Nch-1 may be directly connected to the wiring 3 without fuse 4 as shown in Fig. 6.

As stated above, according to the first to fifth embodiments, the input circuit of the chip comprises the electrostatic protection elements which are connected to the wiring through fuses and have the chip capacity divided by the number of chips. Since the fuses predetermined by the number of chips mounted in a package are disconnected, when a plurality of the chips having such disconnected fuses are mounted in a package, the multi-chip package meets the specified input pin capacity.

Also, when the chip is used for the single chip package, all the electrostatic protection elements may be used without disconnecting any fuses. Accordingly, the semiconductor chip can be used for both the multi-chip package and the single chip package.

In Fig. 10, according to the sixth embodiment, the chip capacity is divided by the number of m or the lowest common multiple of the numbers of o and p, which are the numbers of the chips supposed to be mounted in a package. By doing so, a semiconductor chip useful for a plurality of multi-chip packages can be produced.

When the chips are used commonly for, for example, two multi-chip packages, o-chip package (chips in the number of o are mounted in a package) and p-chip package (chips in the number of p are mounted in a package), the chip capacity of the input pin capacity is divided by the number of m, which is the lowest common multiple of the numbers of o and p. That is, the junction area for

producing the capacity equal to that of the conventional transistors Pch and Nch for the single chip package is divided equally by the number of m. Accordingly, the junction areas of the respective transistors Pch-1 to Pch-m and Nch-1 to Nch-m are 1/m of the junction area of the transistors Pch and Nch, respectively, for the single chip package.

The transistors Pch-1 and Nch-1 forming the first electrostatic protection element 1 are directly connected to the wiring 3. The remaining transistors Pch-2 to Pch-m and Nch-2 to Nch-m forming the second to m-th electrostatic protection elements 1 are connected to the wiring 3 through fuses 4.

When the semiconductor chip having the above structure is used in the single chip package (SCP), one chip is mounted in a package without disconnecting any fuse 4 so that all the electrostatic protection elements 1 in the number of m shown by an arrow A (from the first to m-th electrostatic protection elements 1) are electrically connected to the wiring 3.

When the chips in the number of o are mounted in a multi-chip package, the fuses 4 for the first to m/o-th electrostatic protection elements 1 shown by an arrow B are not disconnected and the fuses 4 for the (m/o + 1)th to m-th electrostatic protection elements 1 are disconnected.

When the chips in the number of p are mounted in a multi-chip package, the fuses 4 for the first to m/p-th electrostatic protection elements 1 shown by an arrow C are not disconnected and the fuses 4 for the (m/p + 1)th to m-th electrostatic protection elements 1 are disconnected.

More specifically, if o is two and p is three, m is six. Accordingly, when the chips in the number of o or two chips are mounted, the fuses 4 for the first to third electrostatic protection elements 1 are not disconnected

and the fuses 4 for the fourth to sixth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-3 and Nch-1 to Nch-3 are used. When the chips in the number of p or three chips are mounted, the fuses 4 for the first to second electrostatic protection elements 1 are not disconnected and the fuses 4 for the third to sixth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-2 and Nch-1 to Nch-2 are used.

In Fig. 11, an input circuit according to the seventh embodiments has the same structure as in the sixth embodiment except that the transistors Pch-1 and Nch-1 forming the first electrostatic protection element 1 are connected to the wiring 3 through fuses 4.

When the semiconductor chip having the above structure is used in the single chip package (SCP), one chip is mounted in a package without disconnecting any fuse 4 so that all the electrostatic protection elements 1 in the number of m shown by an arrow A (from the first to m-th electrostatic protection elements 1) are electrically connected to the wiring 3.

When the chips in the number of o are mounted in a multi-chip package, the fuses 4 for the first to m/o-th electrostatic protection elements 1 shown by an arrow B are not disconnected and the fuses 4 for the (m/o + 1)th to m-th electrostatic protection elements 1 are disconnected.

When the chips in the number of p are mounted in a multi-chip package, the fuses 4 for the first to m/p-th electrostatic protection elements 1 shown by an arrow C are not disconnected and the fuses 4 for the (m/p + 1)th to m-th electrostatic protection elements 1 are disconnected.

In the sixth embodiment, the numbers of the chips which are expected to be mounted in a package are o and p.

In the eight embodiment, the numbers of the chips which are expected to be mounted in a package are o, p, and q.

In Fig. 12, according to the eight embodiment, the chip capacity is divided into the number of m, which is the lowest common multiple of o, p, and q so as to produce a chip commonly used for an o-chip package (in which the chips in the number of o are mounted), p-chip package, and q-chip package.

That is, the junction area for producing the capacity equal to that of the conventional transistors Pch and Nch for the single chip package is divided equally into the number of m. Accordingly, the junction areas of the respective transistors Pch-1 to Pch-m and Nch-1 to Nch-m are 1/m of the junction area of the transistors Pch and Nch, respectively, for the single chip package.

The transistors Pch-1 and Nch-1 forming the first electrostatic protection element 1 are directly connected to the wiring 3. The other transistors Pch-2 to Pch-m and Nch-2 to Nch-m forming the second to m-th electrostatic protection elements 1 are connected to the wiring 3 through fuses 4.

When the semiconductor chip having the above structure is used in the single chip package (SCP), one chip is mounted in a package without disconnecting any fuse 4 so that all the electrostatic protection elements 1 in the number of m shown by an arrow A (from the first to m-th electrostatic protection elements 1) are electrically connected to the wiring 3.

When the chips in the number of o are mounted in a multi-chip package, the fuses 4 for the first to m/o-th electrostatic protection elements 1 shown by an arrow B are connected and the fuses 4 for the (m/o + 1)th to m-th electrostatic protection elements 1 are disconnected.

When the chips in the number of p are mounted in a multi-chip package, the fuses 4 for the first to m/p-th electrostatic protection elements 1 shown by an arrow C are connected and the fuses 4 for the (m/p + 1)th to m-th electrostatic protection elements 1 are disconnected.

When the chips in the number of q are mounted in a multi-chip package, the fuses 4 for the first to m/q-th electrostatic protection elements 1 shown by an arrow D are connected and the fuses 4 for the (m/q + 1)th to m-th electrostatic protection elements 1 are disconnected.

More specifically, if o is two, p is three, and q is four, then m is twelve. Accordingly, when the chips in the number of o or two chips are mounted, the fuses 4 for the first to sixth electrostatic protection elements 1 are connected and the fuses 4 for the seventh to twelfth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-6 and Nch-1 to Nch-6 are used.

When the chips in the number of p or three chips are mounted, the fuses 4 for the first to fourth electrostatic protection elements 1 are connected and the fuses 4 for the fifth to twelfth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-4 and Nch-1 to Nch-4 are used.

When the chips in the number of q or four chips are mounted, the fuses 4 for the first to third electrostatic protection elements 1 are connected and the fuses 4 for the fourth to twelfth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-3 and Nch-1 to Nch-3 are used.

In Fig. 13, an input circuit according to the ninth embodiments has the same structure as in the eighth embodiment except that the transistors Pch-1 and Nch-1

forming the first electrostatic protection element 1 are connected to the wiring 3 through fuses 4.

The chip capacity is divided into the number of m, which is the lowest common multiple of o, p, and q so as to produce a chip commonly used for an o-chip package (package in which the chips in the number of o are mounted), p-chip package(package in which the chips in the number of p are mounted), and q-chip package (package in which the chips in the number of q are mounted).

That is, the junction area for producing the capacity equal to that of the conventional transistors Pch and Nch for the single chip package is divided equally into the number of m. Accordingly, the junction areas of the respective transistors Pch-1 to Pch-m and Nch-1 to Nch-m are 1/m of the junction area of the transistors Pch and Nch, respectively, for the single chip package.

The respective transistors Pch-1 to Pch-m and Nch-1 to Nch-m forming the second to m-th electrostatic protection elements 1 are connected to the wiring 3 through fuses 4.

When the semiconductor chip having the above structure is used in the single chip package (SCP), one chip is mounted in a package without disconnecting any fuse 4 so that all the electrostatic protection elements 1 in the number of m shown by an arrow A (from the first to m-th electrostatic protection elements 1) are electrically connected to the wiring 3.

When the chips in the number of o are mounted in a multi-chip package, the fuses 4 for the first to m/o-th electrostatic protection elements 1 shown by an arrow B are connected and the fuses 4 for the (m/o + 1)th to m-th electrostatic protection elements 1 are disconnected.

When the chips in the number of p are mounted in a multi-chip package, the fuses 4 for the first to m/p-th

electrostatic protection elements 1 shown by an arrow C are connected and the fuses 4 for the (m/p + 1)th to m-th electrostatic protection elements 1 are disconnected.

When the chips in the number of q are mounted in a multi-chip package, the fuses 4 for the first to m/q-th electrostatic protection elements 1 shown by an arrow D are connected and the fuses 4 for the (m/q + 1)th to m-th electrostatic protection elements 1 are disconnected.

More specifically, if o is two, p is three, and q is four, m is twelve. Accordingly, when the chips in the number of o or two chips are mounted, the fuses 4 for the first to sixth electrostatic protection elements 1 are connected and the fuses 4 for the seventh to twelfth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-6 and Nch-1 to Nch-6 are used.

When the chips in the number of p or three chips are mounted, the fuses 4 for the first to fourth electrostatic protection elements 1 are connected and the fuses 4 for the fifth to twelfth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-4 and Nch-1 to Nch-4 are used.

When the chips in the number of q or four chips are mounted, the fuses 4 for the first to third electrostatic protection elements 1 are connected and the fuses 4 for the fourth to twelfth electrostatic protection elements 1 are disconnected so that only the transistors Pch-1 to Pch-3 and Nch-1 to Nch-3 are used.

As described above, according to the present invention, since the input pin capacity of the multi-chip package is set at the same value as that of the single chip package, the specification of the input pin capacity is met and a semiconductor chip can be used commonly for the single chip and multi-chip packages.